

FIG. 1

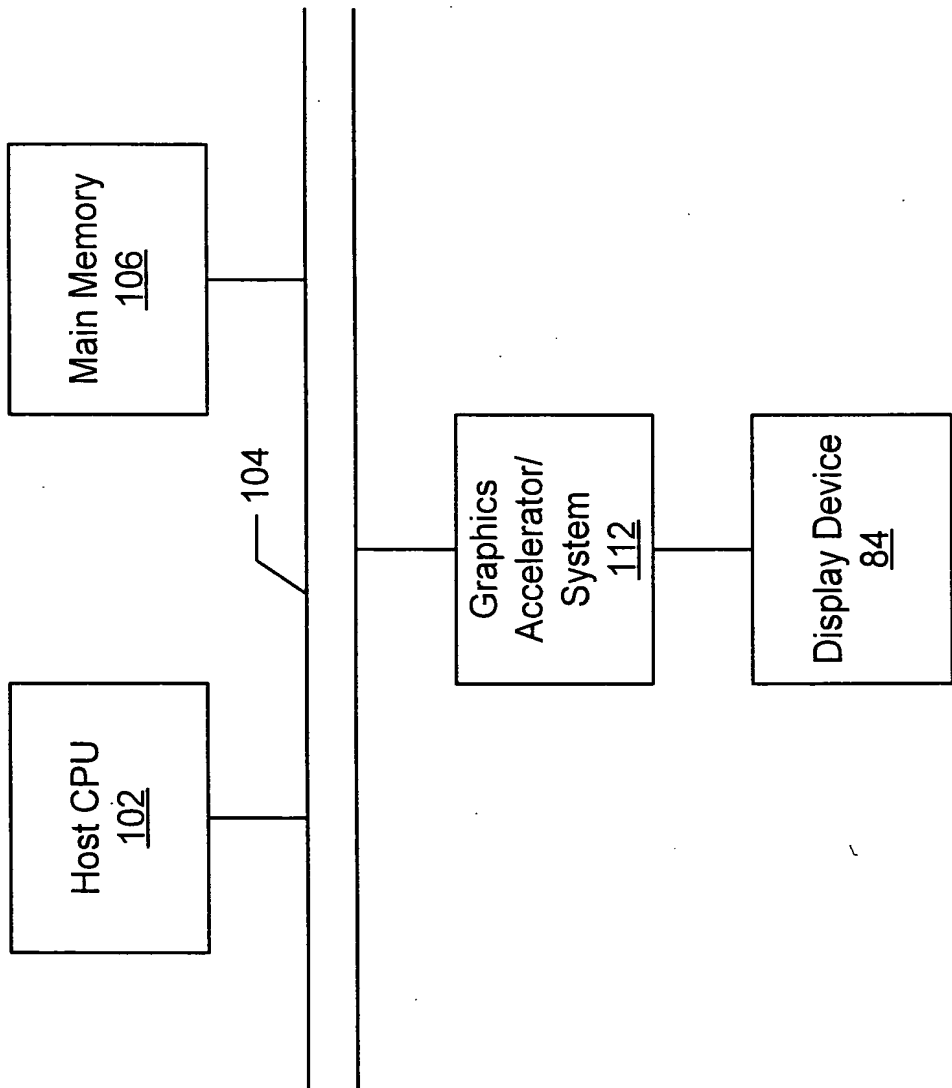


FIG. 2

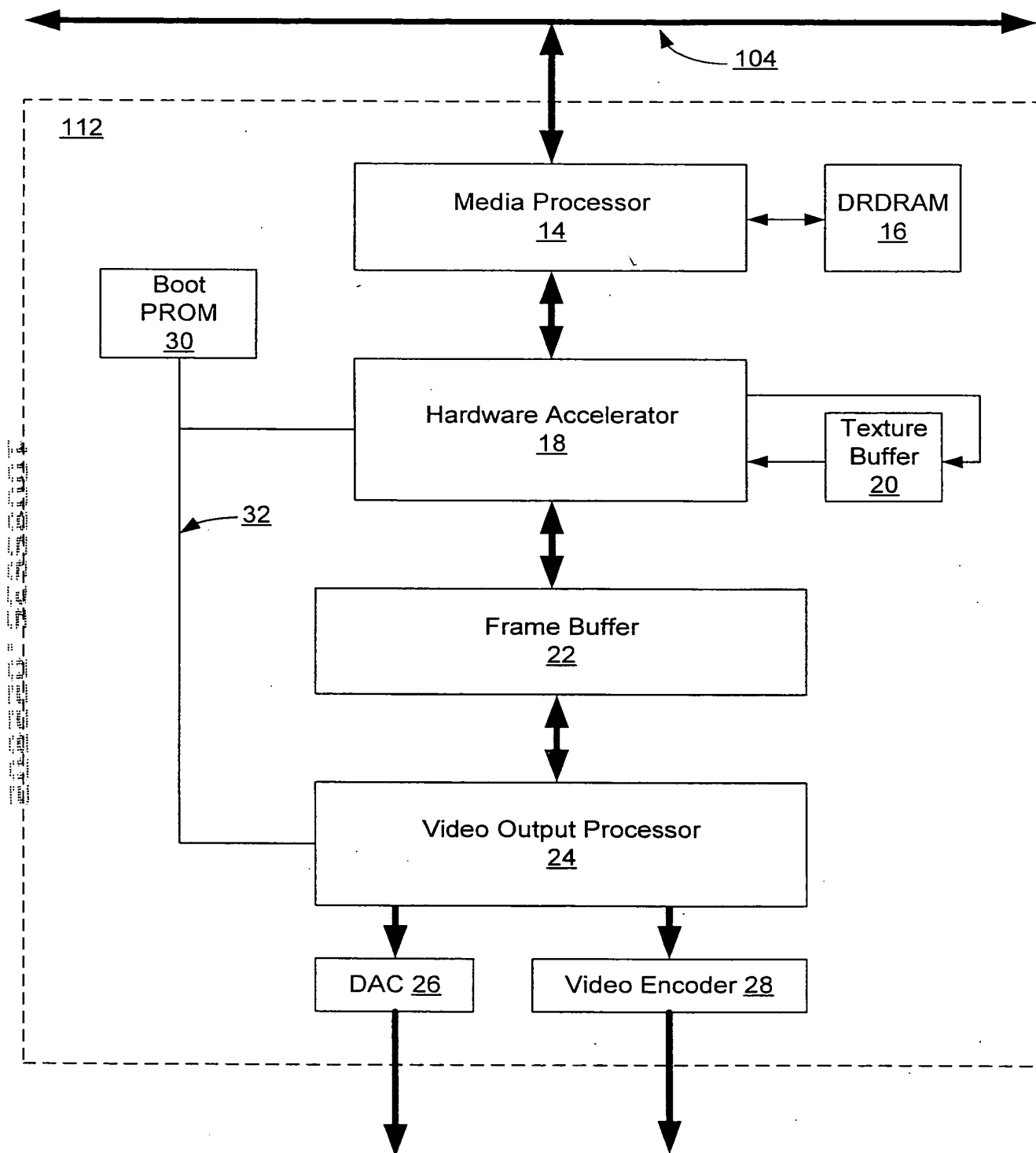


FIG. 3

FIG. 4 is a block diagram of a system 14, according to one embodiment of the present invention.

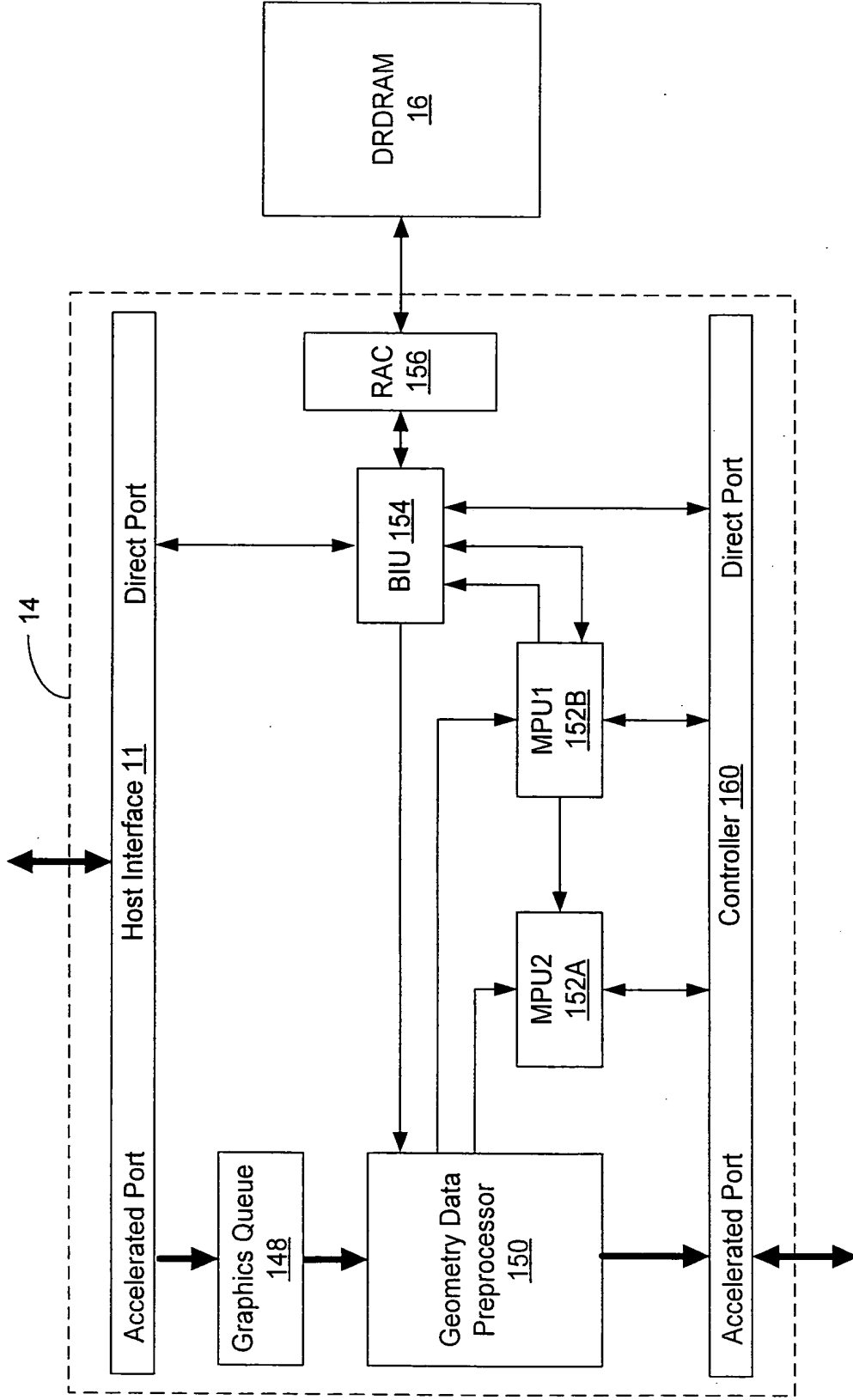


FIG. 4

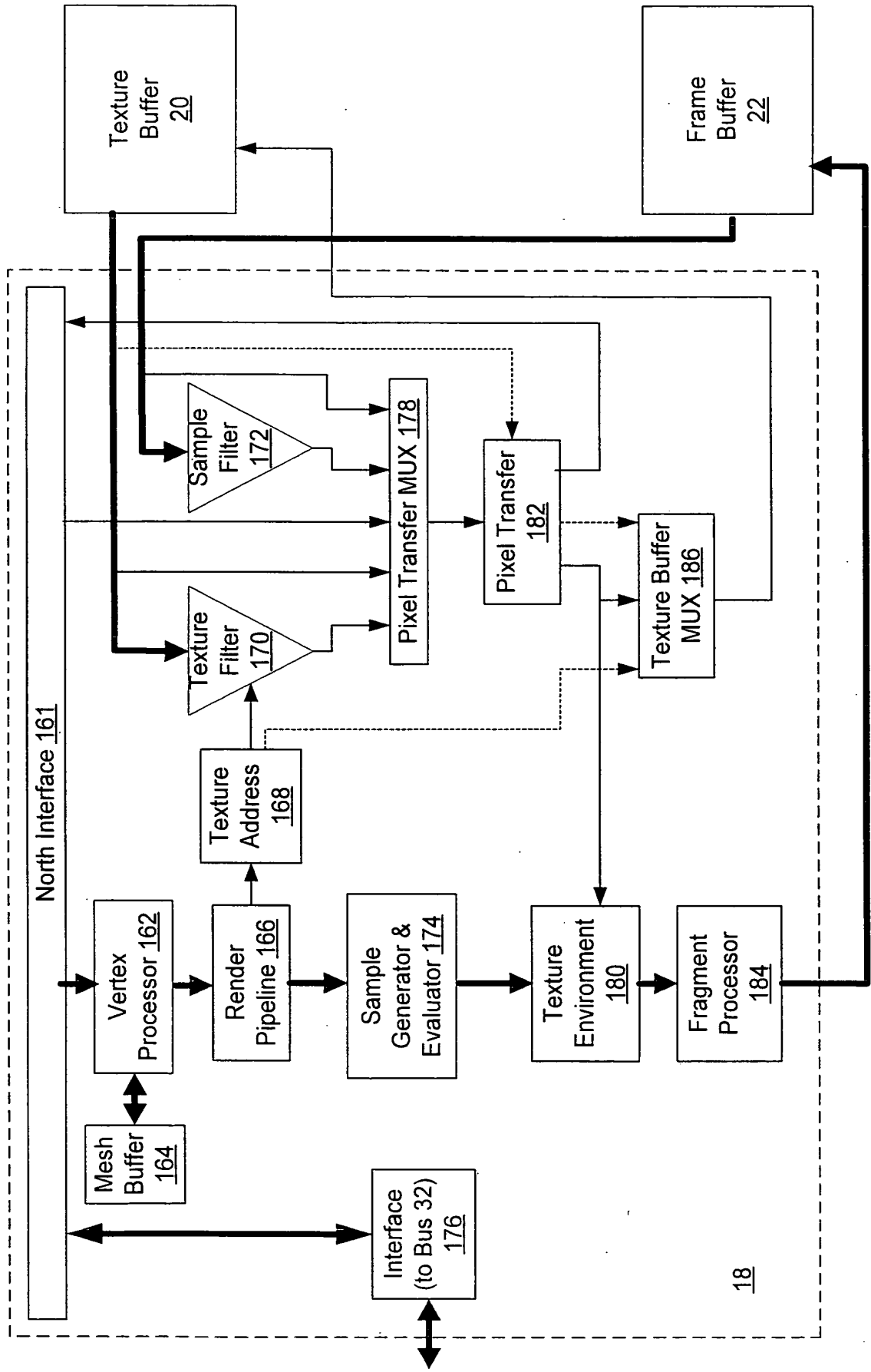


FIG. 5

FIG. 6 is a block diagram of a video output processor 24, showing the internal components and their interconnections. The processor 24 is enclosed in a dashed box and includes a Frame Buffer 22, WLUTs 192, Transparency/Overlay 190, GLUT CLUTs Cursor 194, RasterGen 196A, RasterGen 196B, DAC 26, and Encoder 28. The Frame Buffer 22 is connected to the WLUTs 192. The WLUTs 192 are connected to the Transparency/Overlay 190 and the GLUT CLUTs Cursor 194. The Transparency/Overlay 190 is connected to the GLUT CLUTs Cursor 194. The GLUT CLUTs Cursor 194 is connected to the RasterGen 196A and RasterGen 196B. The RasterGen 196A and RasterGen 196B are connected to the DAC 26 and Encoder 28. The DAC 26 and Encoder 28 are connected to the output bus 32. The output bus 32 is connected to the Video Output Processor 24.

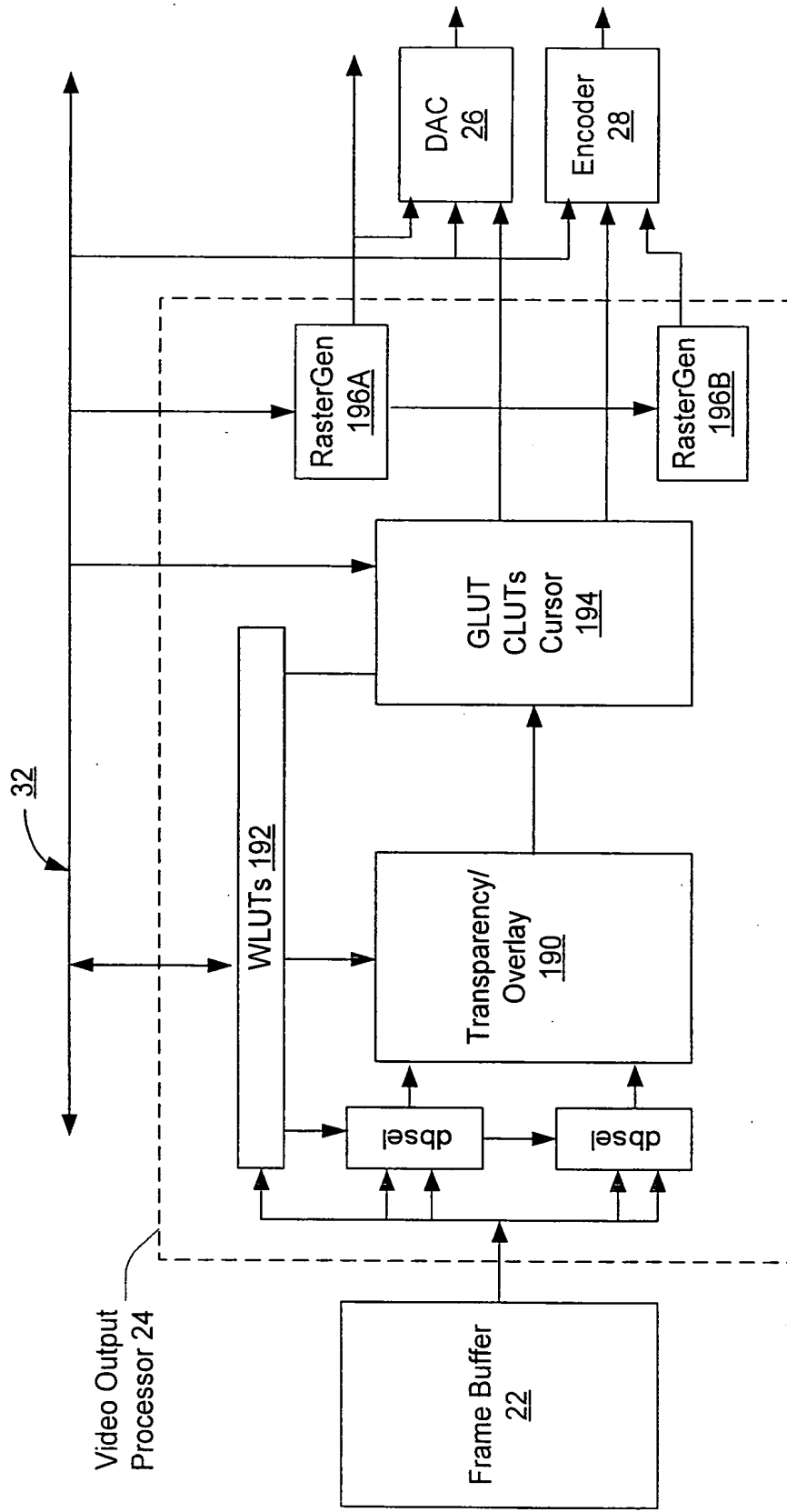
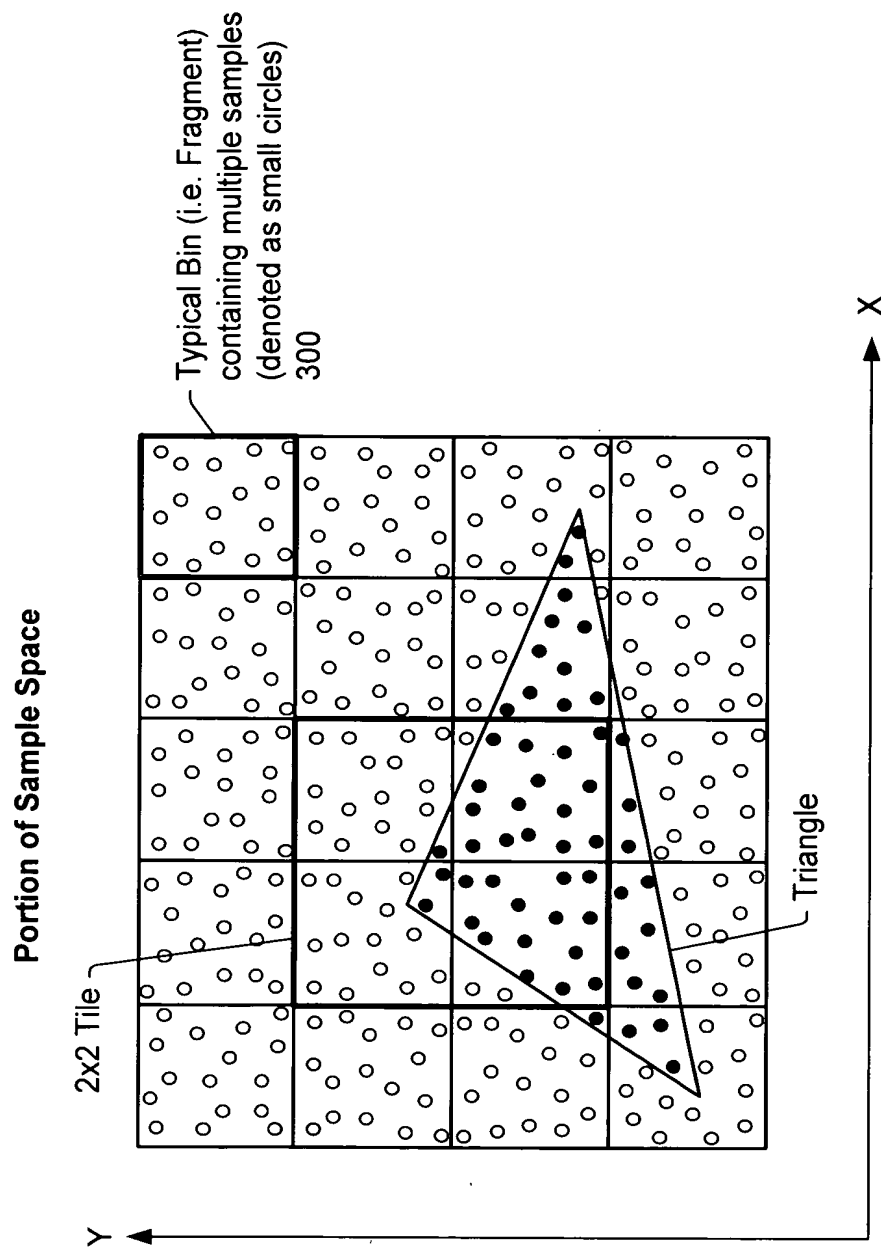


FIG. 6



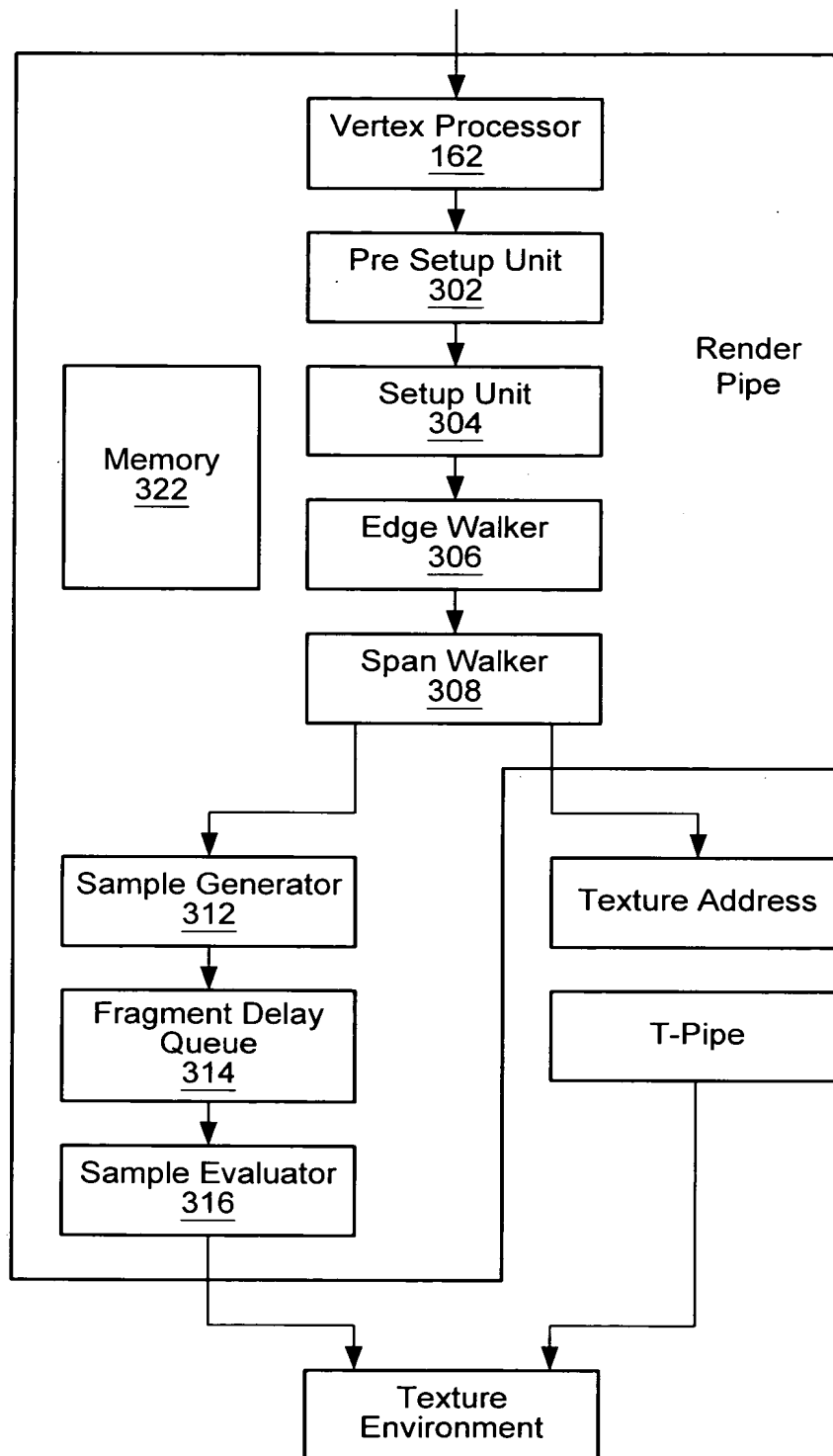


Fig. 8

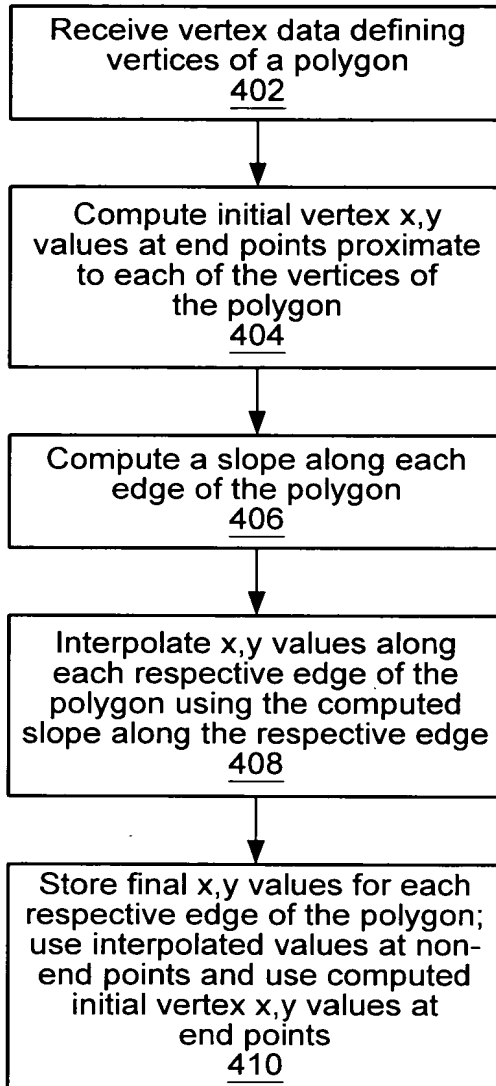


Fig. 9

P_{se}, P_{sm}, P_{me} are the initial edge intercepts

The diagram shows a triangle with vertices M , E , and S . The horizontal axis is labeled $x\text{-major}$ and the vertical axis is labeled $y\text{-major}$. The origin is at vertex S . The point E is on the $x\text{-major}$ axis. The point M is on the $y\text{-major}$ axis. The line segment SE is labeled controlling edge . The point P_{SE} is on the $x\text{-major}$ axis, and the point P_{SM} is on the $y\text{-major}$ axis. A box contains the text: P_{se}, P_{sm}, P_{me} are the initial edge intercepts.

